## IN THE CLAIMS

1-32. (Canceled)

33. (Original) A vertical transistor, comprising:

a semiconductor substrate comprising an upper surface;

a recess disposed in the upper surface, wherein the recess contains a localized epitaxial semiconductor film comprising more than three monolithic surfaces;

a gate dielectric layer disposed over the localized epitaxial semiconductor film; and

an electrode disposed in the recess over the gate dielectric layer.

34. (Original) The vertical transistor according to claim 33, wherein the electrode has an electrode upper surface that is below the substrate upper surface.

35. (Original) The vertical transistor according to claim 33, further including:

a silicon-deuterium transition layer, or a silicon-hydrogen transition layer, or a silicon-hydrogen-deuterium transition layer disposed between the more than three monolithic surfaces and the gate dielectric layer.

36. (Original) The vertical transistor according to claim 33, wherein the gate dielectric layer is selected from a refractory metal oxide, a thermal oxide, a silicon oxide, a silicon oxynitride, a silicon nitride, a carbon-doped oxide, and combinations thereof.

37. (Original) The vertical transistor according to claim 33, wherein the electrode is doped polysilicon.

38. (Original) The vertical transistor according to claim 33, wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess.

39. (Original) The vertical transistor according to claim 33, wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess; and

wherein the source and drain are bounded in a first dimension by a structure having a minimum photolithographic feature.

40. (Original) The vertical transistor according to claim 33, wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;

wherein the source and drain are bounded in a first dimension by a first STI structure having a first minimum photolithographic feature; and

wherein the source or the drain is bounded in a second dimension by a second STI structure having a second minimum feature dimension that is substantially equal to the first minimum feature dimension.

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→ at least one of

be either or.

41. (Original) The vertical transistor according to claim 33, wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;

wherein the source and drain are bounded by a first STI structure;

wherein the source or the drain is bounded by a second STI structure;

wherein the recess is disposed in the substrate to a first depth; and

wherein the STI structures are disposed in the substrate to a second depth, and wherein the second depth is greater than the first depth.

42. (Original) The vertical transistor according to claim 33, wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;

wherein the N+ doped source and the N+ doped drain are bounded in a first dimension by a first STI structure;

wherein the N+ doped source and the N+ doped drain are bounded in a second dimension by a second STI structure; and

wherein the STI structures are each disposed within a recess including a curvilinear epitaxial film.

43. (Original) An electrical device comprising:

a substrate comprising an upper surface;

an active area disposed in the substrate comprising a source and a drain;

a recess disposed between the source and the drain, wherein the recess comprises a substantially curvilinear bottom profile of epitaxial semiconductive material;

a gate dielectric layer disposed over the epitaxial semiconductive material; and

an electrode disposed over the gate dielectric layer.

44. (Original) The electrical device according to claim 43, wherein the electrode has an electrode upper surface that is below the substrate upper surface.

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45. (Original) The electrical device according to claim 43, further including:

a silicon-deuterium transition layer, or a silicon-hydrogen transition layer, or a silicon-hydrogen-deuterium transition layer disposed between the substantially curvilinear bottom profile of epitaxial semiconductive material and the gate dielectric layer.

46. (Original) The electrical device according to claim 43, wherein the gate dielectric layer is selected from a refractory metal oxide, a thermal oxide, a silicon oxide, a silicon oxynitride, a silicon nitride, a carbon-doped oxide, and combinations thereof.

47. (Original) The electrical device according to claim 43, wherein the electrode is doped polysilicon.

48. (Currently Amended) The electrical device according to claim 43, wherein the substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess; and wherein the source and drain are bounded in a first dimension by a first shallow trench isolation structure comprising a minimum photolithographic feature.

49. (Original) The electrical device according to claim 43, wherein the substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;

wherein the source and drain are bounded in a first dimension by a first shallow trench isolation structure comprising a minimum photolithographic feature; and

wherein the source and the drain are bounded in a second dimension by a second shallow trench isolation structure including the minimum photolithographic feature.

50. (Original) An electrical device comprising:

a monocrystalline semiconductor substrate including an upper surface;

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an active area disposed in the monocrystalline semiconductor substrate including a source and a drain;

a recess disposed between the source and the drain;

wherein the recess includes a substantially curvilinear bottom profile comprising epitaxial semiconductive material;

a gate dielectric layer disposed over the epitaxial semiconductive material in the recess;

an electrode disposed in the recess; and

a first shallow trench isolation (STI) structure disposed in the monocrystalline semiconductor substrate, wherein the recess exposes at least a portion thereof.

51. (Original) The electrical device according to claim 50, further including:

a chip package, wherein the monocrystalline semiconductor substrate is disposed in the chip package; and

a host, wherein the chip package is disposed in the host.

52. (Original) The electrical device according to claim 50, further including:

a chip package, wherein the monocrystalline semiconductor substrate is disposed in the chip package;

a host, wherein the chip package is disposed in the host, wherein the host includes a memory module; and

an electronic system, wherein the memory module is disposed in the electronic system.

53. (Original) The electrical device according to claim 50, further including:

a chip package, wherein the monocrystalline semiconductor substrate is disposed in the chip package;

a host, wherein the chip package is disposed in the host, wherein the host includes a dynamic random access memory module; and

an electronic system, wherein the dynamic random access memory module is disposed in the electronic system.

54. (Original) The electrical device according to claim 50, further including:

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a chip package, wherein the monocrystalline semiconductor substrate is disposed in the chip package;

a host, wherein the chip package is disposed in the host; and

an electronic system, wherein the host is disposed in the electronic system.

55. (Original) The electrical device according to claim 50, further including:

a second STI disposed in the monocrystalline semiconductor substrate in a direction parallel to the first STI.

56. (Original) An electrical device comprising:

a semiconductor substrate including an upper surface;

a recess disposed in the upper surface wherein the recess is covered with a substantially curvilinear bottom profile including epitaxial semiconductive material;

a first gate dielectric layer disposed over the epitaxial semiconductive material;

a floating gate film disposed over the first gate dielectric layer;

a second gate dielectric layer disposed over the floating gate film; and

an electrode disposed over the second gate dielectric layer.

57. (Original) The electrical device according to claim 56, further including:

a first shallow trench isolation (STI) structure disposed immediately adjacent the recess.

58. (Original) The electrical device according to claim 56, further including:

a first shallow trench isolation (STI) structure disposed immediately adjacent the recess; and

a second STI structure disposed in the semiconductor substrate in a direction parallel to the first STI.

59. (Original) The electrical device according to claim 56, further including:

a chip package, wherein the semiconductor substrate is disposed in the chip package; and

a host, wherein the chip package is disposed in the host.

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60. (Original) The electrical device according to claim 56, further including:

a chip package, wherein the monocrystalline semiconductor substrate is disposed in the chip package;

a host, wherein the chip package is disposed in the host, wherein the host comprises a chip set; and

an electronic system, wherein the chip set is disposed in the electronic system.

61. (Original) A computer system, comprising:

a processor;

a memory system coupled to the processor;

an input/output (I/O) circuit coupled to the processor and the memory system; and

a vertical transistor disposed in the processor, the vertical transistor including:

a semiconductor substrate comprising an upper surface;

a recess disposed in the upper surface, wherein the recess contains an epitaxial semiconductor film comprising more than three monolithic surfaces;

a gate dielectric layer disposed over the epitaxial semiconductor film; and

an electrode disposed in the recess over the gate dielectric layer.

62. (Original) The computer system according to claim 61, wherein the processor is disposed in a host selected from a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, and an aircraft.

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